LEADING AT THE EDGE

TECHNOLOGY AND MANUFACTURING DAY
10 NM TECHNOLOGY LEADERSHIP

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KEY MESSAGES

- Intel’s 10 nm process technology has the world’s tightest transistor & metal pitches along with hyper scaling features for leadership density.

- Intel’s 10 nm technology is a full generation ahead of other “10 nm” technologies.

- Enhanced versions of Intel 10 nm provide improved power/performance within the 10 nm process family.

- Hyper scaling extracts the full value of multi-patterning schemes and allows Intel to continue the benefits of Moore’s Law economics.
AGENDA

- Intel 10 nm Features
- Intel 10 nm Hyper Scaling
- Enhanced Versions of Intel 10 nm
- Hyper Scaling Redux
**10 nm Hyper Scaling**

<table>
<thead>
<tr>
<th>Fin Pitch</th>
<th>Min Metal Pitch</th>
<th>Cell Height</th>
<th>Gate Pitch</th>
</tr>
</thead>
<tbody>
<tr>
<td>42 nm</td>
<td>52 nm</td>
<td>399 nm</td>
<td>70 nm</td>
</tr>
<tr>
<td>14 nm</td>
<td>14 nm</td>
<td>14 nm</td>
<td>14 nm</td>
</tr>
<tr>
<td>34 nm</td>
<td>36 nm</td>
<td>272 nm</td>
<td>54 nm</td>
</tr>
<tr>
<td>.81x</td>
<td>.69x</td>
<td>.68x</td>
<td>.78x</td>
</tr>
</tbody>
</table>

10 nm features aggressive pitch scaling - world’s first Self-Aligned Quad Patterning
10 nm aggressive scaling & new features deliver 2.7x transistor density improvement
Intel 10 nm hyper scaling features result in Transistor Density above 100MTr/mm²

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
10 nm Fins are ~25% taller and ~25% more closely spaced than 14 nm
Intel's 10 nm technology features a Fin Pitch of 34 nm, Fin Height of 53 nm.
Intel's 10 nm technology features 54 nm gate pitch

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
Intel 10 nm Gate Pitch is the tightest in the industry

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.
Metal Pitch Scaling

Intel 10 nm technology features a minimum metal pitch of 36 nm

World’s first Self-Aligned Quad Patterning

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
Intel 10 nm technology has the tightest minimum metal pitch in the industry.

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
Contact over active gate is a revolutionary feature for another ~10% area scaling.
Process innovations enable denser single dummy gate at cell borders
Single dummy gate at cell borders provides ~20% effective area scaling benefit.
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Fin pitch and metal pitch scaling allow cell height to scale 0.68x from 14 nm

Source: Intel
Cell height and gate pitch scaling provides traditional area reduction of $\sim 0.5x$. 

Source: Intel
Intel 10 nm hyper scaling features further improve area scaling to 0.37x
10 nm hyper scaling features provides better-than-normal 0.37x logic area scaling

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
Intel 10 nm hyper scaling features provide ~2.7x transistor density improvement

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
Hyper scaling maintains the rate of Moore’s Law density scaling

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
**LOGIC TRANSISTOR DENSITY**

Intel 10 nm is a full generation ahead of other “10 nm” technologies

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.
10 nm offers a range of SRAM cells for density and power/performance

SRAM cell area scaled ~0.6x from 14 nm

Source: Intel
Hyper scaling delivers better microprocessor die area scaling than the normal trend.
AGENDA

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10 nm enhancements improve performance and extend technology life

Source: Intel. 2017-2021 are estimates based upon current expectations and available information.
10 nm technology continues trend of power/performance improvements

Source: Intel estimates based upon current expectations and available information.
**TECHNOLOGY ENHANCEMENTS**

10++ enhancements offer improved power/performance within 10 nm generation

Source: Intel estimates based upon current expectations and available information.
TECHNOLOGY ENHANCEMENTS

High Q Inductors

High Res Substrates

High Voltage FinFETs

Precision Resistors

Low Cost
Dense
High Perf

Interconnect Options

Intel's 10 nm technology family has features for a broad range of products

Source: Intel
AGENDA

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Hyper scaling allows Intel to continue the economics of Moore’s Law
- More than 2X logic transistor density increase but with longer than 2 year cadence
- Same rate of transistor density increase as traditional Moore’s Law scaling
- Same rate of Cost per Transistor improvement as traditional Moore’s Law scaling
- Power/performance enhancements within each process node

Why hyper scaling?
- Multi-pass patterning adds to the cost of lithography
- Hyper scaling extracts the full cost per transistor benefit of advanced patterning schemes

Hyper scaling would not be possible without Self-Aligned Dual and Self-Aligned Quad Patterning along with other 10 nm hyper scaling innovations
Hyper scaling allows the economics of Moore’s Law to continue

Source: Intel estimates based upon current expectations and available information.
CONCLUSIONS

- Intel’s 10 nm process technology has the world’s tightest transistor & metal pitches along with hyper scaling features for leadership density
- Intel’s 10 nm technology is a full generation ahead of other “10 nm” technologies
- Enhanced versions of Intel 10 nm provide improved power/performance within the 10 nm process family
- Intel’s 10nm process technology is on track to commence manufacturing in 2H’17
- Hyper scaling extracts the full value of multi-patterning schemes and allows Intel to continue the economic benefits of Moore’s Law

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.
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