LEADING AT THE EDGE
TECHNOLOGY AND MANUFACTURING DAY
MOORE’S LAW LEADERSHIP

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Intel Technology and Manufacturing Day 2017 occurs during Intel's “Quiet Period,” before Intel announces its 2017 first quarter financial and operating results. Therefore, presenters will not be addressing first quarter information during this year's program.

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Intel leads the industry in introducing innovations that enable scaling

Hyper scaling on Intel 14 nm and 10 nm provides better-than-normal scaling while continuing to reduce cost per transistor

Intel's 14 nm technology has ~3 year lead over other “10 nm” technologies with similar logic transistor density

Intel’s 10 nm technology provides industry-leading logic transistor density using a quantitative density metric

Enhanced versions of 14 nm and 10 nm provide improved performance and extend the life of these technologies

Moore’s Law is alive and well at Intel

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.
Intel leads the industry by at least 3 years in introducing major process innovations.
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Intel innovation leadership

Intel leads the industry by at least 3 years in introducing major process innovations.

Intel: 90nm, 65nm, 45nm, 32nm, 22nm, 14nm, 10nm


Others: 90nm, 65nm, 40nm, 28nm, 20nm, 16nm, 10nm

Strained Silicon, High-k Metal Gate, Self Align Via, FinFET Transistor, Hyper Scaling

Intel leads the industry by at least 3 years in introducing major process innovations.
Intel leads the industry by at least 3 years in introducing major process innovations.
Intel developed all the major logic process innovations used by our industry over the past 15 years.

Source: Intel. 10 nm is based upon current expectations and available information.
INDUSTRY RECOGNITIONS

2008 SEMI AWARD FOR NORTH AMERICA
“For integration of strain-enhanced mobility techniques for CMOS transistors”

2012 SEMI AWARD FOR NORTH AMERICA
“For the first development, integration and introduction of a successful high-k dielectric and metal electrode gate stack for CMOS IC production”

2015 SEMI AWARD FOR NORTH AMERICA
“For implementation of bulk CMOS FinFET production”

2016 IEEE CORPORATE INNOVATION AWARD
“For pioneering the use of high-k metal gate and tri-gate transistor technologies in high-volume manufacturing”
Traditional logic area scaling was $\sim 0.49x$ per generation using a “gate pitch x cell height” metric.
... but “gate pitch x cell height” is not a comprehensive transistor density metric

<table>
<thead>
<tr>
<th>Logic Area Metric</th>
<th>Logic Cell Width</th>
<th>Logic Cell Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>45nm</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>32nm</td>
<td>.49x</td>
<td></td>
</tr>
<tr>
<td>22nm</td>
<td>.45x</td>
<td></td>
</tr>
</tbody>
</table>

HVM Wafer Start Date

- 45nm: 2007
- 32nm: 2010
- 22nm: 2013

Source: Intel
Logic Transistor density metric

Standard NAND+SFF metric is a more accurate estimate of logic transistor density

\[
0.6 \times \frac{\text{NAND2 Tr Count}}{\text{NAND2 Cell Area}} + 0.4 \times \frac{\text{Scan Flip Flop Tr Count}}{\text{Scan Flip Flop Cell Area}} = \text{# Transistors / mm}^2
\]
Logic transistor density improvement was ~2.2x per generation using NAND+SFF metric

Source: Intel
14 nm hyper scaling provided ~2.5x transistor density improvement

Source: Intel
10 nm hyper scaling provides ~2.7x transistor density improvement

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
Transistor density improvements continue at a rate of ~doubling every 2 years

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
Logic node names should be accompanied with logic transistor density.

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
Other measured transistor densities using same NAND+SFF metric

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.
Rate of density improvement was slow on other 20/16/14 nm technologies

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.
Intel 14 nm has ~1.3x higher transistor density than other 20/16/14 nm

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.
Other “10 nm” technologies will have density similar to Intel 14 nm, but ~3 years later.

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.
Logic node names should be accompanied with logic transistor density
MOORE’S LAW IS A LAW OF ECONOMICS

LOWER COST
Same circuitry in half the space (Feature Neutral)

MOORE COST SAVINGS

OR

MORE FUNCTIONALITY (more transistors)
Twice the number of transistors in same space

MOORE PERFORMANCE
Normal microprocessor die area scaling has been ~0.62x per generation
Microprocessor Die Area Scaling

Hyper scaling delivers 0.46-0.43x die area scaling on 14 nm and 10 nm.

Source: Intel.
Normal scaling would have provided poor CPT improvements

Source: Intel.
Normal scaling + 450 mm wafers would have provided better CPT

Source: Intel.
Hyper scaling on Intel 14 nm and 10 nm provides lower CPT.
Scaled transistors continue to provide improved performance and lower power.

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
14 nm enhancements improve performance and extend technology life

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
10 nm enhancements improve performance and extend technology life

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
## Derivative Technologies

### Device Options

<table>
<thead>
<tr>
<th>Technology</th>
<th>CPU</th>
<th>SoC</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Perf Transistors</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Low Leakage Transistors</td>
<td></td>
<td>Yes</td>
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<tr>
<td>Analog/RF Transistors</td>
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<td>Yes</td>
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<tr>
<td>HV I/O Transistors</td>
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<td>Yes</td>
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<tr>
<td>High-Q Inductors</td>
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<td>Yes</td>
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<tr>
<td>Precision Resistors</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>MIMCAP</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

### Interconnect Stack Options

- **Low Cost**
- **Dense**
- **High Perf**

**Multiple derivative options offered for each technology generation**

Source: Intel
Wide range of 14 nm products in volume production on various derivative technologies
HETEROGENEOUS INTEGRATION OPTIONS

- Multi-Chip Package
  - Die 1
  - Die 2
  - Package Substrate
  - Poor density of die-package connections
  - Poor density of die-die interconnects

- Interposer
  - Die 1
  - Die 2
  - Package Substrate
  - Good density of die-interposer connections
  - Good density of die-die interconnects
  - Higher cost of large interposer + thru-silicon vias

- Embedded Multi-Die Interconnect Bridge
  - Die 1
  - Die 2
  - Silicon Bridge
  - Package Substrate
  - Good density of die-bridge connections
  - Good density of die-die interconnects
  - Low cost of small silicon bridges

EMIB technology provides high density, high bandwidth die-die interconnects
EMIB technology provides high density, high bandwidth die-die interconnects.
**EMBEDDED MULTI-DIE INTERCONNECT BRIDGE**

55 um pitch bumps

Silicon Bridge

130 um pitch bumps

Silicon Die
EMBEDDED MULTI-DIE INTERCONNECT BRIDGE

55 um pitch bumps

130 um pitch bumps

Silicon Bridge

Silicon Die
EMIB enables dense and cost effective in-package heterogeneous integration
KEY MESSAGES

- Intel leads the industry in introducing innovations that enable scaling
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