2019 INVESTOR MEETING

PRODUCT LEADERSHIP

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Chief Engineering Officer, Intel
Group President, TSCG
Statements in this presentation that refer to business outlook, future plans and expectations are forward-looking statements that involve a number of risks and uncertainties. Words such as "anticipates," "expects," "intends," "goals," "plans," "believes," "seeks," "estimates," "continues," "may," "will," "would," "should," "could," and variations of such words and similar expressions are intended to identify such forward-looking statements. Statements that refer to or are based on estimates, forecasts, projections, uncertain events or assumptions, including statements relating to total addressable market (TAM) or market opportunity, future products and the expected availability and benefits of such products, and anticipated trends in our businesses or the markets relevant to them, also identify forward-looking statements. Such statements are based on management’s expectations as of May 8, 2019, unless an earlier date is indicated, and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in these forward-looking statements. Important factors that could cause actual results to differ materially from the company's expectations are set forth in Intel's earnings release dated April 25, 2019, which is included as an exhibit to Intel's Form 8-K furnished to the SEC on such date. Additional information regarding these and other factors that could affect Intel's results is included in Intel's SEC filings, including the company's most recent reports on Forms 10-K and 10-Q. Copies of Intel's Form 10-K, 10-Q and 8-K reports may be obtained by visiting our Investor Relations website at www.intc.com or the SEC's website at www.sec.gov.

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DATA GROWTH AND OPPORTUNITY

DATA-CENTRIC PRODUCT LEADERSHIP

PRODUCT HIGHLIGHTS
DRIVING FORCE OF DATA-CENTRIC TRANSFORMATION

**DIGITAL DATA GENERATED**

- PRODUCTIVITY DATA
- BROADCAST MEDIA
- WEB / MOBILE
- IOT / ANALYTICS

**DATA-CENTRIC TRANSITIONS**

- **COMPUTE DIVERSITY**
  - Scalar, vector, spatial - AI, graphics, media, analytics

- **NETWORK CLOUDIFICATION**
  - Compute & storage distributed across core, access, and edge networks

- **INTELLIGENT AGENTS**
  - Proliferation of autonomous / AI-enabled devices, things, and edge gateways

**WEB / MOBILE**

- Outbound/Structured
- Inbound/Unstructured/Latency Sensitive

**IOT / ANALYTICS**

- Structured
- Unstructured/Latency Sensitive

**CAGR (17-25)**

- 20%
- 35%

Source: Analyst reports, tech press, industry interviews
DATA-CENTRIC TRANSITIONS DRIVE GROWTH

**DATA CENTRIC:** ~$220B

**PC CENTRIC:** ~$68B

HIGH GROWTH SEGMENTS
2018-23 growth relative to aggregate TAM

- **DATACENTER**
  - DC FPGA
  - AI
  - NVMe SSD

- **NETWORK**
  - NFV/SDN
  - 5G

- **IOT**
  - Edge Comp.
  - ADAS/AD

- **PC AND ADJACENCIES**
  - Gaming
  - Modem
  - Notebook
  - Chrome

Source: Intel calculated 2023 TAM and growth rates derived from analyst forecasts and Intel TAM model.
PRODUCT LEADERSHIP EVOLUTION: SIX PILLARS OF INNOVATION

PC-CENTRIC ERA
CPU LEADERSHIP, TRANSISTOR SCALING

DATA-CENTRIC ERA
WORKLOAD-OPTIMIZED PLATFORMS, EFFORTLESS CUSTOMER & DEVELOPER INNOVATION

SIX CONCURRENT PILLARS OF INNOVATION
ACCELERATING PRODUCT ROADMAP REFRESH
Data-centric workloads require scalar, vector, matrix and spatial compute: xPUs

- SW portability, reusability and performance grows in value with compute diversity
- Confidentiality, integrity and resiliency become increasingly critical
- Increased data movement makes interconnects critical to the platform
- Memory bandwidth/latency/cost critical to handle data
- Compute diversity benefits from process and packaging diversity
PROCESS TECHNOLOGY & PACKAGING

**PC-CENTRIC**
TRANSISTOR SCALING & MONOLITHIC INTEGRATION

One process design point for all products
Monolithic integration
Product restricted by reticle

**DATA-CENTRIC**
HETEROGENEOUS PROCESSES & INTEGRATION

Multiple processes optimized for individual IPs
Multi-chip integration with advanced packaging
Product unconstrained by reticle
Transistor efficiency
(Perf / W)

Most ambitious scaling in history
- 2.7x density scaling
- Self-aligned Quad-patterning
- Contact Over Active Gate
- Cobalt Interconnect (M0, M1)
- 1st Gen Foveros 3D Stacking
- 2nd Gen EMIB

Transistor efficiency (Perf / W)

LEARNINGS

Balance between schedule, performance, power, cost
14NM INTRA-NODE ENHANCEMENTS

Transistor efficiency
(Perf / W)

LEARNINGS
Balance between schedule, performance, power, cost
Significant opportunity for intra-node advancement
Balance between schedule, performance, power, cost

Significant opportunity for intra-node advancement

Value in maintaining mix of nodes

Ease-of-design accelerates innovation
Transistor efficiency (Perf / W)

- 2x scaling
- Planned intra-node optimizations
- 4x Reduction in design rules
- EUV
- Next-gen Foveros & EMIB packaging
Transistor efficiency (Perf / W)

- 14
- 14+
- 14++
- 10
- 10+
- 10++
- 7
- 7+
- 7++

- 1272
- 1274
- 1276

One ML of scaling & performance start of node + one ML performance intra-node

Multi-chip SoC construction for non-compromise performance

Radical design simplification accelerates innovation

10nm shipping in June, multiple products through 2019 and 2020

7nm progressing to plan

Lead product launch in 2021
10nm Ice Lake Client
Shipping in June

APPORX.

- 2X Graphics Performance
- 2.5X - 3X AI Performance
- 2X Video Encode
- 3X Wireless Speeds

Disclaimer: Results are approximate and have been estimated or simulated as of April 2019 using Intel internal analysis or architecture simulation or modeling.

- Graphics and video – Next Gen Graphics Iris Plus Experience
- Wireless – Intel’s Wi-Fi 6 (GIG+) vs typical competitive 11AC design
- AI – AIXPRT Community 2 Preview; OpenVINO 2018.R5, Max Throughput 15W WHL to 15W ICL projection

For more complete information about performance and benchmark results, visit www.intel.com/benchmarks. Performance results are based on testing as of date specified and may not reflect all publicly available security updates. See configuration disclosure for details. No product or component can be absolutely secure.
10nm Ice Lake Client
Shipping in June

Multiple Product Launches
Across Entire Portfolio Through 2019 and 2020

Xeon CPU | GP-GPU | AI Inference
FPGA | 5G/Networking | ...
Xe Architecture-Based GP-GPU using Foveros for Datacenter AI & HPC

Launch in 2021
For every order of magnitude performance from new hardware, there is >2 orders of magnitude unlocked by software

Raja Koduri
Chief Architect, SVP
Intel Architecture, Graphics and Software
INTEL SOFTWARE MAGNITUDE

Example 1: Java runtime optimizations
Example 2: Persistent memory complete stack optimizations

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Example 3: Deep Learning Boost

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SOFTWARE - COMPETITIVE DIFFERENTIATOR

Per core performance advantage

- Web Browsing (1.7x)
- Productivity (1.6x)
- Networking (2.0x)
- Gaming (1.4x)
- Content Creation (2.5x)
- Java (2.1x)
- Data Analytics (1.9x)
- High Performance Compute (1.9x)
- Deep Learning (10.3x)

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Software Leadership

>15,000 software engineers

#1 contributor to Linux kernel;
>1/2 million lines of code modified each year

>100 operating systems optimized

top three contributors to Chromium OS

>10,000 high touch customer deployments

top 10 contributor to Openstack

>12 million developers

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12 million developers
DATA CENTRIC DEVELOPER GROWTH

One Architecture

Cloud Native

8 million developers

GPU

1 million developers

AI

100K developers

12 million developers
DATA CENTRIC DEVELOPER GROWTH
“The future is a diverse mix of Scalar, Vector, Matrix and Spatial architectures deployed in CPU, GPU, FPGA and Accelerator sockets...”

*Intel Arch day, Dec '2018*
DATA CENTRIC DEVELOPER GROWTH
DATA CENTRIC DEVELOPER GROWTH
INTEL VS. COMPETITORS

Interconnect

Memory

CPU | GPU

AI | FPGA

PC

Network

Data Center

Competitor 1

GPU

Cloud

PC

GPU

Competitor 2

CPU

GPU
simple and scalable
open
one developer experience
oneAPI

Coming soon to a developer near you in Q4 2019
PRODUCT LEADERSHIP ACROSS WIDE DESIGN SPECTRUM

Data Center  Network  Intelligent Agents
# Compute Diversity

## 2nd Gen Intel® Xeon Scalable Processors

### World Record + Real Workload Performance Leadership

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<th>Software</th>
<th>Intel® MKL-DNN (AI)</th>
<th>OpenVINO (AI)</th>
<th>SPDK (Storage)</th>
<th>DPDK (Network)</th>
<th>Intel® Security Libraries - DC</th>
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<tr>
<td>Security</td>
<td>Intel® OPTANE DC™ Memory Encryption</td>
<td>Intel® Threat Detection Tech</td>
<td>Intel® SGX Card</td>
<td>Intel® select* DPM (Power Management)</td>
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<td>Interconnect</td>
<td>Ultra Path Interconnect</td>
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<tr>
<td>Memory</td>
<td>Intel® OPTANE DC™ Highest Native DDR Bandwidth</td>
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<tr>
<td>XPU Architectures</td>
<td>Intel® AVX-512</td>
<td>Intel® Speed Select</td>
<td>Intel® DL Boost</td>
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<tr>
<td>Process &amp; Packaging</td>
<td>14nm Scaling</td>
<td>56C MCP</td>
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</table>

**Up to 28X AI performance**

**Up to 56 core per socket, 112 core in two socket**

**Up to 200GB/s bandwidth per socket**

**Up to 36TB addressable memory**

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For more complete information about performance and benchmark results, visit www.intel.com/benchmarks. Performance results are based on testing as of date specified and may not reflect all publicly available security updates. No product or component can be absolutely secure.
INTELLIGENT AGENTS

LAKEFIELD

PACKAGE

PC in Mobile form factor – 12x12x1
Chipset
Power Delivery
Ultra low power logic - P1222
INTELLIGENT AGENTS

LAKEFIELD

FOVEROS

BASE

PACKAGE

Scalable 3D silicon interconnect
Ultra low-power: 0.15 pico Joules / bit
High bandwidth: 2-3X 2.5D interposer
Scalable power delivery: 3W-1KW
High yield process for die stacking
INTELLIGENT AGENTS
LAKEFIELD

**INTELLIGENT AGENTS**

**LAKEFIELD**

**COMPUTE**

10 nm process compute
Hybrid architecture: Core + Atom
Thermal solution to enable 3D stacking
INTELLIGENT AGENTS
LAKEFIELD

POP DRAM integration with 1 mm Z-height
<table>
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<th>Category</th>
<th>Features</th>
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<tr>
<td>Software</td>
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<td>UFS 3.0 USB 3.0 MIPI CSI2</td>
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<td>Memory</td>
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<td>XPU Architectures</td>
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<td>Hybrid Architecture</td>
<td>Sunny Cove CPU Tremont CPU GEN11 Graphics</td>
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<tr>
<td>Process &amp; Packaging</td>
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</tbody>
</table>

Results have been estimated or simulated as of April, 2019 using internal Intel analysis or architecture simulation or modeling vs. AML product.

Disclaimer: Results are approximate and have been estimated or simulated as of April 2019 using Intel internal analysis or architecture simulation or modeling. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks. Performance results are based on testing as of date specified and may not reflect all publicly available security updates. See configuration disclosure for details. No product or component can be absolutely secure.
SUMMARY

Data drives extraordinary opportunities for growth

Intel products & methods targeted to win data-centric growth with six pillar innovation model

You will see this in our product leadership
**CONFIGURATION DISCLOSURE**

Performance results are based on testing as of dates shown in configuration and may not reflect all publicly available security updates. See configuration disclosure for details. No product or component can be absolutely secure. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYMark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit www.intel.com/benchmarks.

Approx. 3x Ice Lake Wireless Speeds: 802.11ax 2x2 160MHz enables 2402Mbps maximum theoretical data rates, ~3X (2.8X) faster than standard 802.11ac 2x2 80MHz (867Mbps) as documented in IEEE 802.11 wireless standard specifications, and require the use of similarly configured 802.11ax wireless network routers.

Approx. 2x Ice Lake Video Encode: Based on 4k HEVC to 4k HEVC transcode (8bit). Intel preproduction system, ICL 15w compared to WHL 15w. Measured by Intel as of April 2019.

Approx. 2x Ice Lake Graphics Performance: Workload: 3DMark11 v 1.0.132. Intel PreProduction ICL U4+2 15W Configuration (Assumptions); Processor: Intel® Core™ i7 (ICL-U 4+2) PL1=15W TDP, 4C8T, Memory: 2x8GB LPDDR4-3733 2Rx8, Storage: Intel® 760p m.2 PCIe NVMe SSD with AHCI Microsoft driver, Display Resolution: 3840x2160 eDP Panel 12.5", OS: Windows® 10 RS5-17763.316, Graphics driver: PROD-H-RELEASES_ICL-PV-2019-04-09-1006832. Vs config – Intel PreProduction WHL U4+2 15W Configuration (Measured), Processor: Intel® Core™ i7-8565U (WHL-U4+2) PL1=15W TDP, 4C8T, Turbo up to 4.6Ghz, Memory: 2x8GB DDR4-2400 2Rx8, Storage: Intel® 760p m.2 PCIe NVMe SSD with AHCI Microsoft driver, Display Resolution: 3840x2160 eDP Panel 12.5", OS: Windows® 10 RS4-17134.112, Gfx driver: 100.6195. Measured by Intel as of April 2019.

Approx. 2.5x-3x Ice Lake AI Performance: Workload: images per second using AIXPRT Community Preview 2 with Int8 precision on ResNet-50 and SSD-Mobilenet-v1 models. Intel preproduction system, ICL-U, PL1 15w, 4C/8T, Turbo TBD, Intel Gen11 Graphics, GFX driver preproduction, Memory 8GB LPDDR4X-3733, Storage Intel SSD Pro 760P 256GB, OS Microsoft Windows 10, RS5 Build 17763.316, preprod bios. Vs. Config – HP spectre x360 131t 13-ap0038nr, Intel® Core™ i7-8565U, PL1 20w, 4C/8T, Turbo up to 4.6Ghz, Intel UHD Graphics 620, Gfx driver 26.20.100.6709, Memory 16GB DDR4-2400, Storage Intel SSD 760p 512GB, OS – Microsoft Windows 10 RS5 Build 17763.316, preprod bios. Measured by Intel as of April 2019.
2nd Gen Intel® Xeon Scalable Processors up to 28X AI Performance: Based on Intel internal testing: 28x performance improvement based on Intel® Optimization for Café ResNet-50 inference throughput performance on Intel® Xeon® Scalable Processor.

28x inference throughput improvement on Intel® Xeon® Platinum 9282 processor with Intel® DL Boost: Tested by Intel as of 2/26/2019. Platform: Dragon rock 2 socket Intel® Xeon® Platinum 9282(56 cores per socket), HT ON, turbo ON, Total Memory 768 GB (24 slots/ 32 GB/ 2933 MHz), BIOS:SE5C620.86B.00.01.0241.112020180249, Centos 7 Kernel 3.10.0-957.5.1.el7.x86_64, Deep Learning Framework: Intel® Optimization for Caffe version: https://github.com/intel/caffe d554cb1, ICC 2019.2.187, MKL DNN version: v0.17 (commit hash: 830a10059a018cd2634d94195140cf2d8790a75a), model: https://github.com/intel/caffe/blob/master/models/intel_optimized_models/int8/resnet50_int8_full_conv.prototxt, BS=64, No datalayer syntheticData:3x224x224, 56 instance/2 socket, Datatype: INT8 vs. Tested by Intel as of July 11th 2017: 2S Intel® Xeon® Platinum 8180 CPU @ 2.50GHz (28 cores), HT disabled, turbo disabled, scaling governor set to "performance" via intel_pstate driver, 384GB DDR4-2666 ECC RAM. CentOS Linux release 7.3.1611 (Core), Linux kernel 3.10.0-514.10.2.el7.x86_64, SSD: Intel® SSD DC S3700 Series (800GB, 2.5in SATA 6Gb/s, 25nm, MLC).Performance measured with: Environment variables: KMP_AFFINITY='granularity=fine,compact', OMP_NUM_THREADS=56, CPU Freq set with cpupower frequency-set -d 2.5G -u 3.8G -g performance. Caffe: (http://github.com/intel/caffe/), revision f96b759f71b2268135f690af267158b92b150b5c. Inference measured with "caffe time --forward_only" command, training measured with "caffe time" command. For "ConvNet" topologies, synthetic dataset was used. For other topologies, data was stored on local storage and cached in memory before training. Topology specs from https://github.com/intel/caffe/tree/master/models/intel_optimized_models (ResNet-50). Intel C++ compiler ver. 17.0.2 20170213, Intel MKL small libraries version 2018.0.20

Performance results are based on testing as of 2/26/2019 (28x) and may not reflect all publically available security updates. No product can be absolutely secure. See configuration disclosure for details.
Approx. 10x Lakefield Standby SoC Power Improvement: Estimated or simulated as of April 2019 using Intel internal analysis or architecture simulation or modeling. Vs. Amber Lake.

Approx. 1.5x-2x Lakefield Active SoC Power Improvement: Estimated or simulated as of April 2019 using Intel internal analysis or architecture simulation or modeling. Workload: 1080p video playback. Vs. Amber Lake next-gen product.

Approx. 2x Lakefield Graphics Performance: Estimated or simulated as of April 2019 using Intel internal analysis or architecture simulation or modeling. Workload: GfxBench. LKF 5W & 7W Configuration (Assumptions); Processor: LKF PL1=5W & 7W TDP, 5C5T, Memory: 2X4GB LPDDR4x - 4267MHz, Storage: Intel® 760p m.2 PCIe NVMe SSD; LKF Optimized Power configuration uses UFS, Display Resolution: 1920x1080 for Performance; 25x14 eDP 13.3" and 19x12 MIPI 8.0" for Power, OS: Windows® 10 RS5. Power policy set to AC/Balanced mode for all benchmarks except SYSmark 2014 SE which is measured in AC/BAPCo mode for Performance. Power policy set to DC/Balanced mode for power. All benchmarks run in Admin mode., Graphics driver: X.X Vs. Configuration Data: Intel® Core™ AML Y2+2 5W measurements; Processor: Intel® Core™ i7-8500Y processor, PL1=5.0W TDP, 2C4T, Turbo up to 4.2GHz/3.6GHz, Memory: 2x4GB LPDDR3-1866MHz, Storage: Intel® 760p m.2 PCIe NVMe SSD, Display Resolution: 1920x1080 for Performance; 25x14 eDP 13.3" for Power, OS: Windows 10 Build RS3 17134.112. SYSmark 2014 SE is measured in BAPCo power plan. Power policy set to DC/Balanced mode for power. All benchmarks run in Admin mode, Graphics driver: driver.whl.1006167-v2.
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